ATLAS @ LBL

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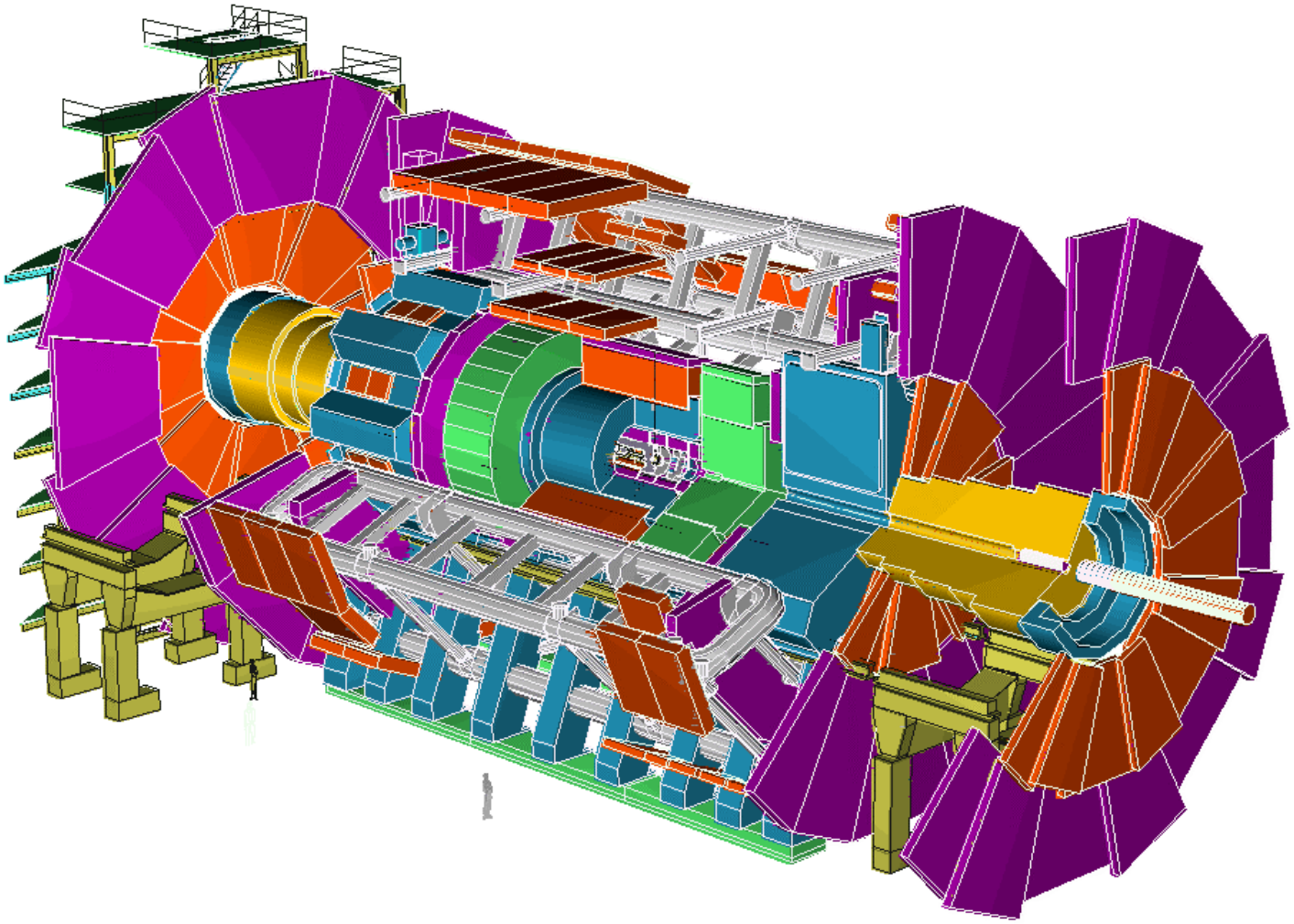
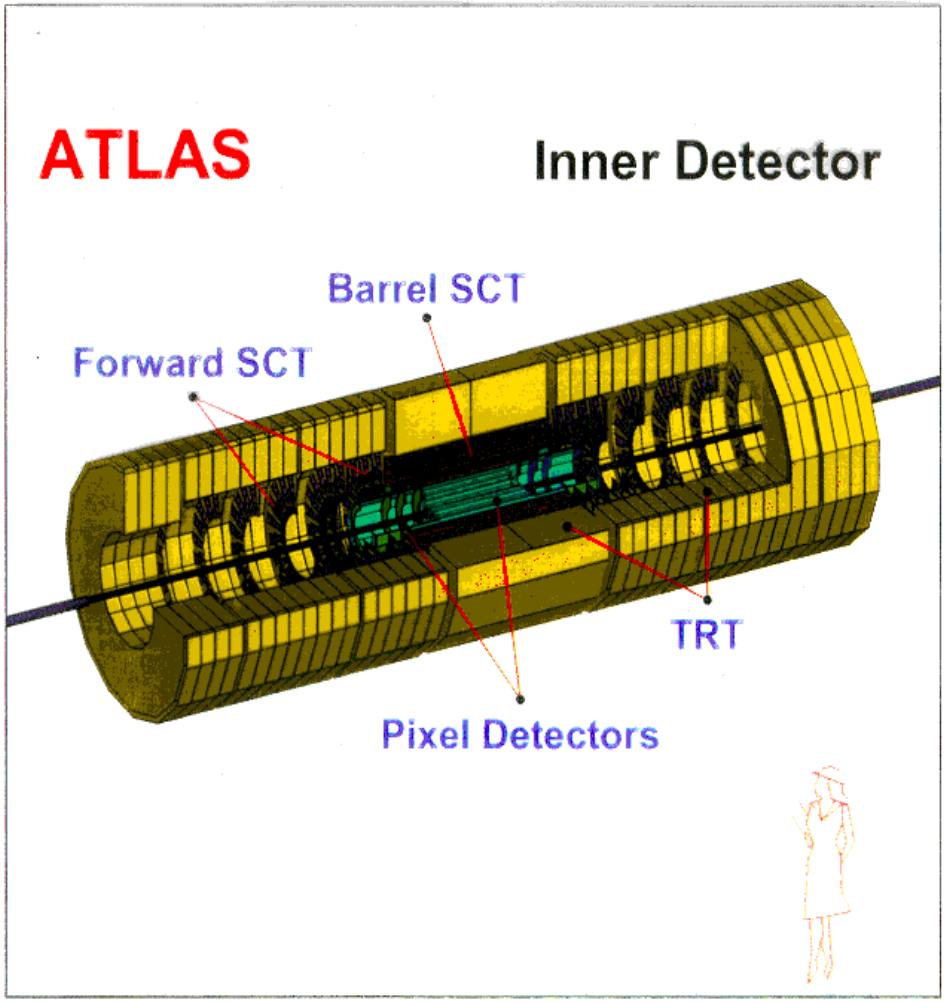
The ATLAS Detector

Physics Division



Inner Detector

- **Pixels**
  - 3 layers+disks
- **Silicon strips**
  - 4 stereo layers+disks
- **Straw Tubes + transition radiator**
  - 36 layers



LBNL and ATLAS

- **Pixel detector system**
  - Development of this new technology - electronics and mechanics
  - Production of about one-third of system
- **Silicon strip detector system**
  - Development of binary readout architecture, integration into modules
  - Production of integrated circuits and testing, and detector modules
- **Software and computing**
  - Development of core software needed for data storage and framework for analysis (Athena)
  - Specific contributions to Inner Tracking Detector software
- **Physics simulation and studies**
  - Coordination of physics simulation codes
  - And use of same to establish computing/software requirements and for physics studies

Collaboration roles

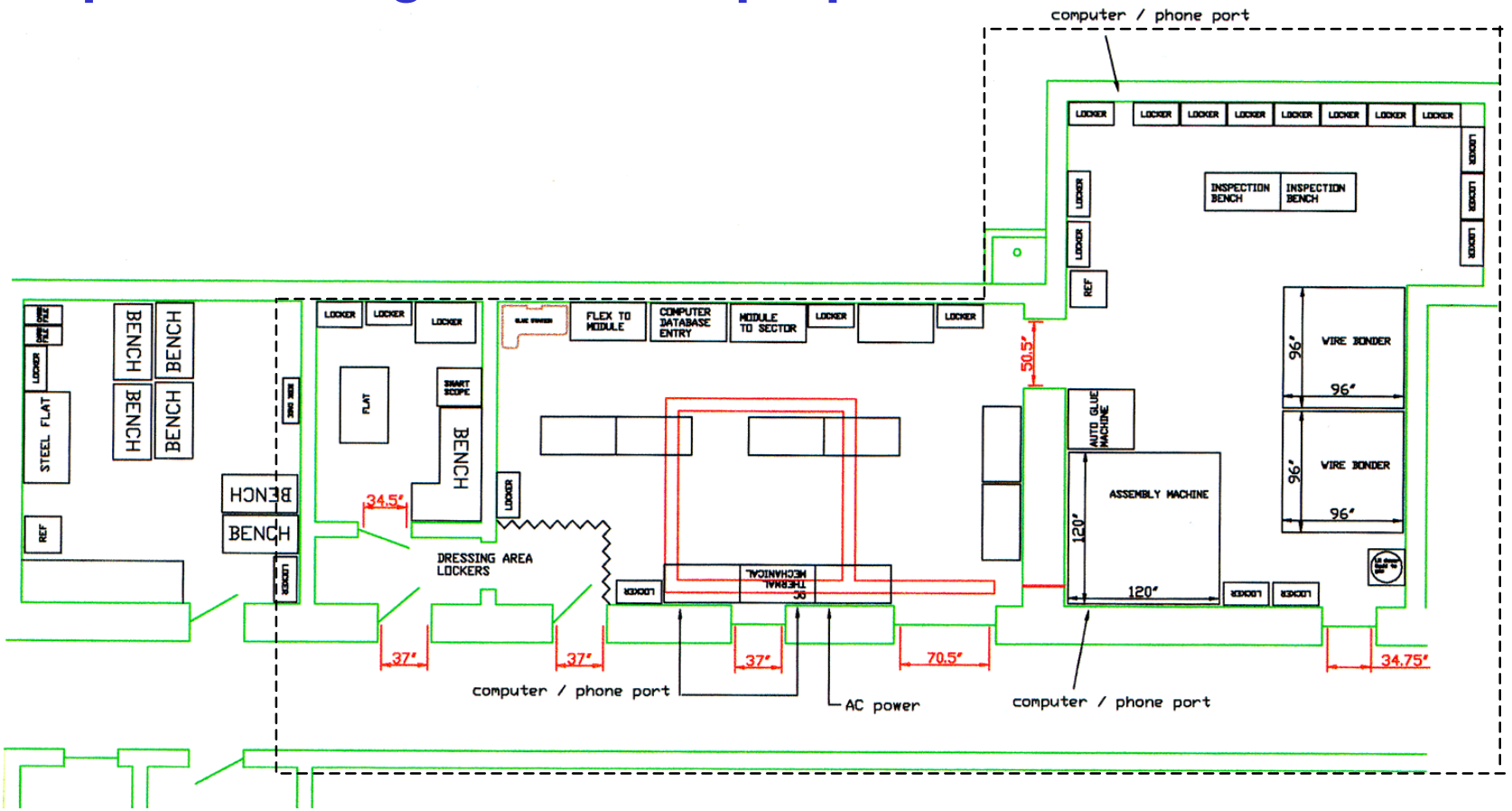
- US Atlas Institution Board Chair: Jim Siegrist
- US Atlas Silicon Subsystem Lead: Gil Gilchriese
- Pixel Electronics Coordinator, Inner Detector Steering Group: Kevin Einsweiler
- US Atlas Physics Manager, Deputy Atlas Physics Coordinator, Monte Carlo Generator Group Leader: Ian Hinchliffe
- SCT Steering Group Member: Carl Haber
- Software Framework Chief Architect: David Quarrie
- US Atlas Education Coordinator: Michael Barnett

What's new?

- US Atlas Pixel baseline review occurred 3-Nov-2000
- New pixel layout - reduced number of disks 5 –> 3, pixel system to be fully insertable in SCT –> leading LBL role in mechanical engineering here
- Deep submicron effort for rad-hard pixel electronics initiated
- SCT readout technologies selected
- LBL IC test system for SCT delivered to CERN 10/00
- Software framework adopted and in development
- New cleanroom assembly area commissioned at LBL
- New people joined:
  - V. Fadeyev SCT electronics
  - M. Garcia-Sciveres Pixel modules
  - open position for post-doc on pixel project

Assembly Space

- Thanks to the Directorate!, space in Bldg. 50 has been renovated to be clean rooms. Work is complete and we have moved in.
- Second space in Bldg. 77 now in preparation.



Atlas clean room construction

Completed assembly areas

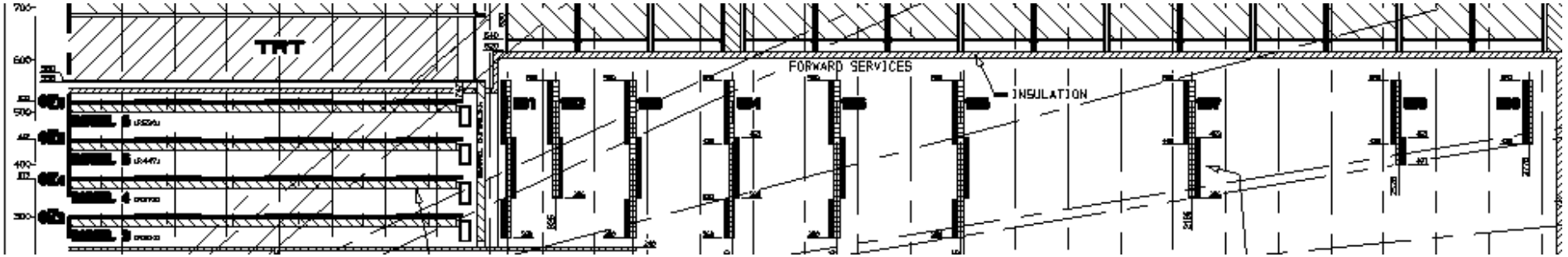
Pixel assembly area with gluing machine visable

Strips assembly area showing vision assisted alignment station

Semiconductor Tracker (SCT)

Physics Division

- **Lots of silicon**
  - **~ 60 m^2**
  - **~ 6 million channels**
  - **Single-sided, p-on-n detectors bonded back-to-back to provide small angle stereo => ~ 4000 modules**
- **Radiation environment is about 10M Rad worst case over lifetime**

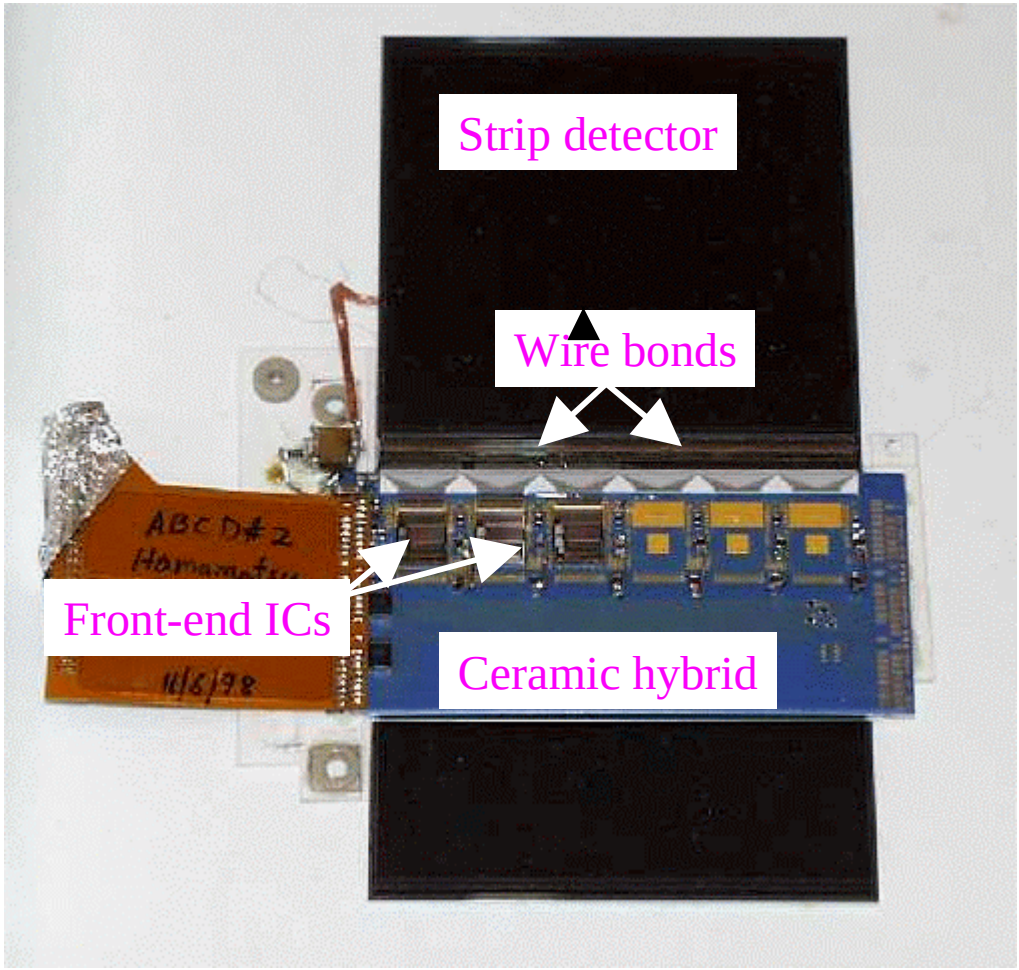


Semiconductor Tracker@LBNL

- LBNL group collaborates closely with SCIPP group at UC Santa Cruz
- LBNL is currently involved in the following aspects of the SCT
  - Integrated circuit testing
  - Hybrid testing
  - Module testing
  - Development of module assembly tooling for production
  - Irradiation of electronics (mostly) and some module components.
- LBNL production responsibilities
  - Integrated circuits test system
  - Irradiation (quality control) of integrated circuits
  - Hybrid assemby and testing
  - Barrel module assembly and testing, ~ 750 modules in 2 years

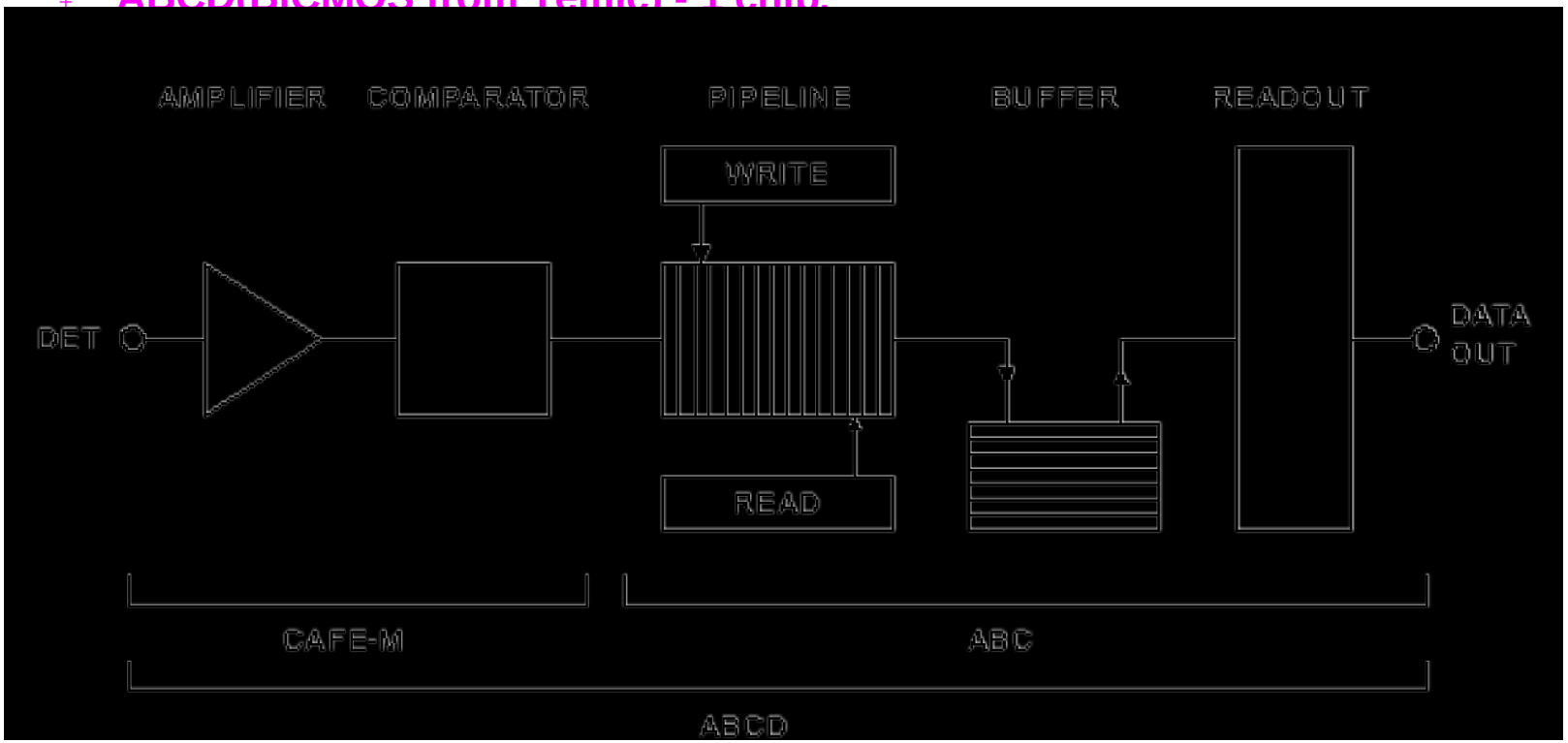
SCT Module

- Modules are the building blocks of the SCT system
- Module consists of 4 detectors, hybrid package, thermal heat spreader and support
- Effort to date has focused on
  - The testing of integrated circuits on hybrids and with detectors attached
  - Completing the precision tooling needed for module assembly
- Moving to pre-production activity



Silicon Strip IC Electronics

- The ATLAS signal processing scheme for silicon strips is based upon a binary hit/no-hit readout
- This approach was pioneered in the US originally for SDC and Zeus..
- Eventually two rad-hard solutions came under development
  - CAFÉ-M(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips..
  - ABCD(BiCMOS from Temic) - 1 chip.



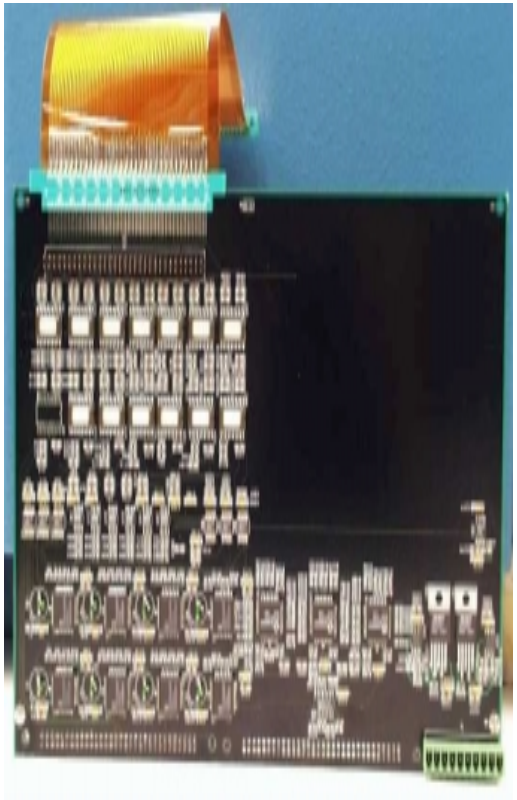
Silicon Strip IC Electronics

- Prototypes of all three ICs were fabricated and tested.
- Initially none met specifications and we contributed to the understanding and redesign of these circuits, in collaboration with UC Santa Cruz, Rutherford Lab and CERN.
- Second prototypes of all circuits were built and tested, and functioned pre-rad.
- Serious low dose rate effects were observed with the bipolar (CAFE) front end.
- The probed yield of the DMILL (ABCD) chip was low and a trim DAC was added to each channel to control threshold spread.
- ATLAS has selected the DMILL (ABCD) chip as the baseline. A new version has been received (August ’00) and is currently under test both at the wafer level (yield) and on modules. Basic function is OK, parts irradiated, module results not available yet.
- Pending final review production lots will be released Spring 2001.
- Low yield and lot to lot consistency remain a concern with the DMILL technology.

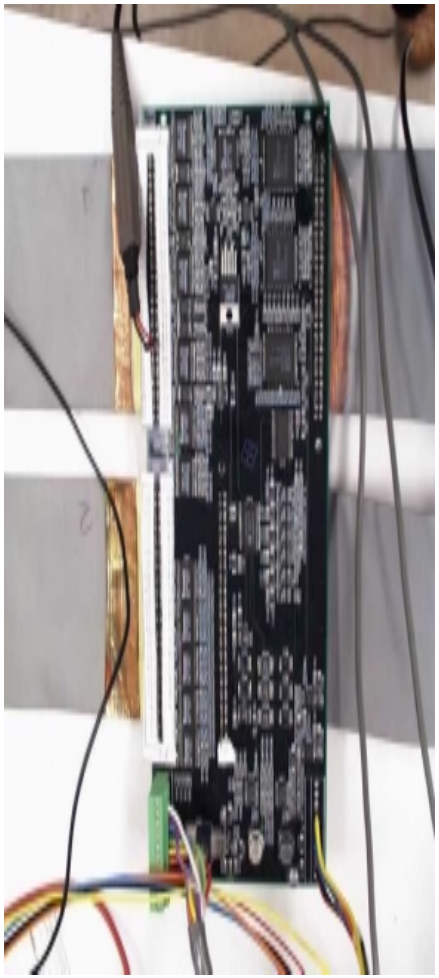
IC Test System

- Developed by A.Ciocio, (H.Niggli), C.Vu, V.Fadeyev, T. Stezelberger, (N.Busek)
- SCT DAQ electronics not sufficient to drive chips while under wafer probe
- LBL system was developed to allow high speed wafer testing and to scan signal height and timing margins.
- The full production lot cannot be scanned without this system in an acceptable time period
- First systems delivered 10/00 to CERN and UCSC for evaluation on new batch of ABCD3 chips.
- LBL to deliver systems to CERN, RAL, and UCSC

IC test system components



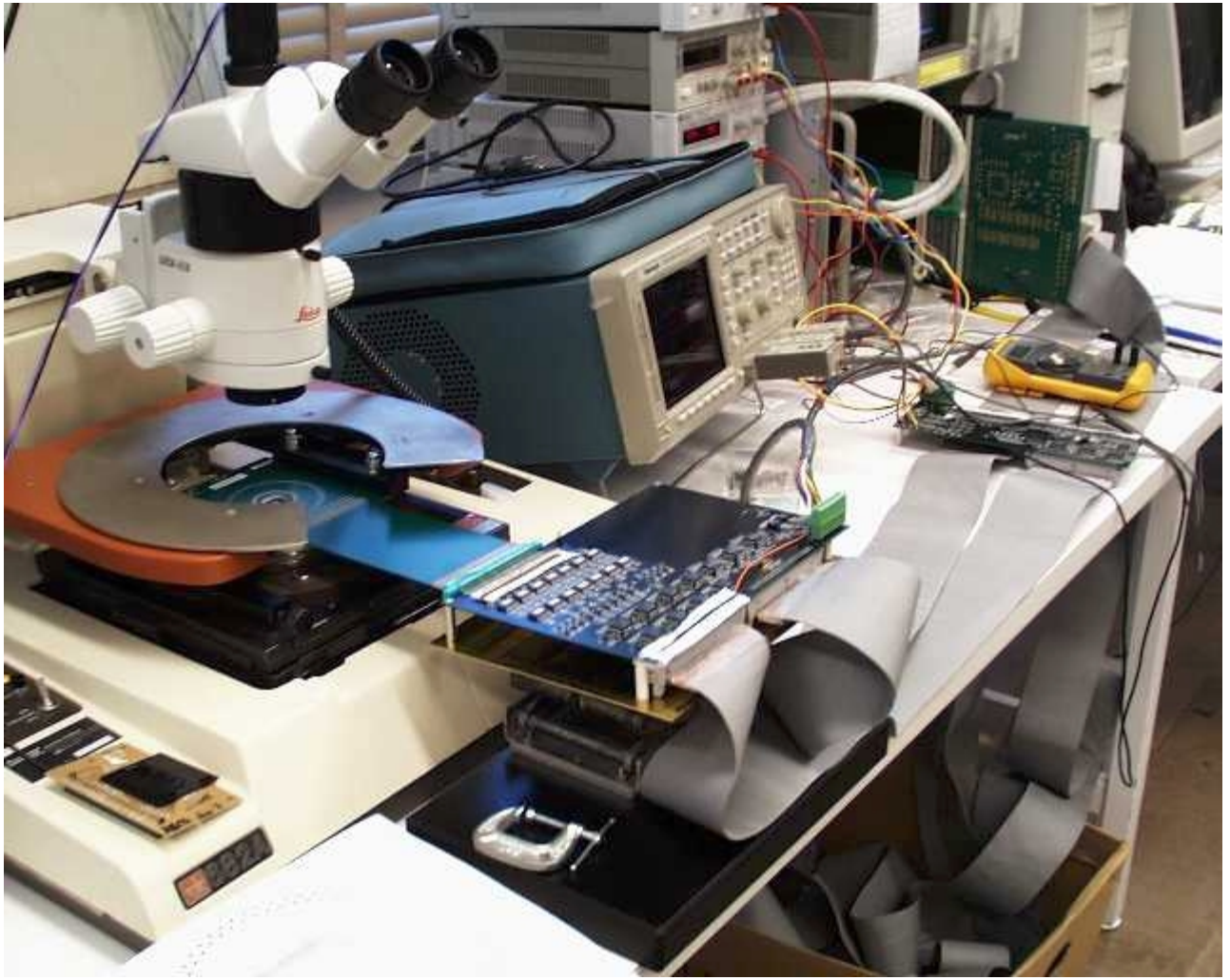
Concard



Pin driver

VME card

IC test system



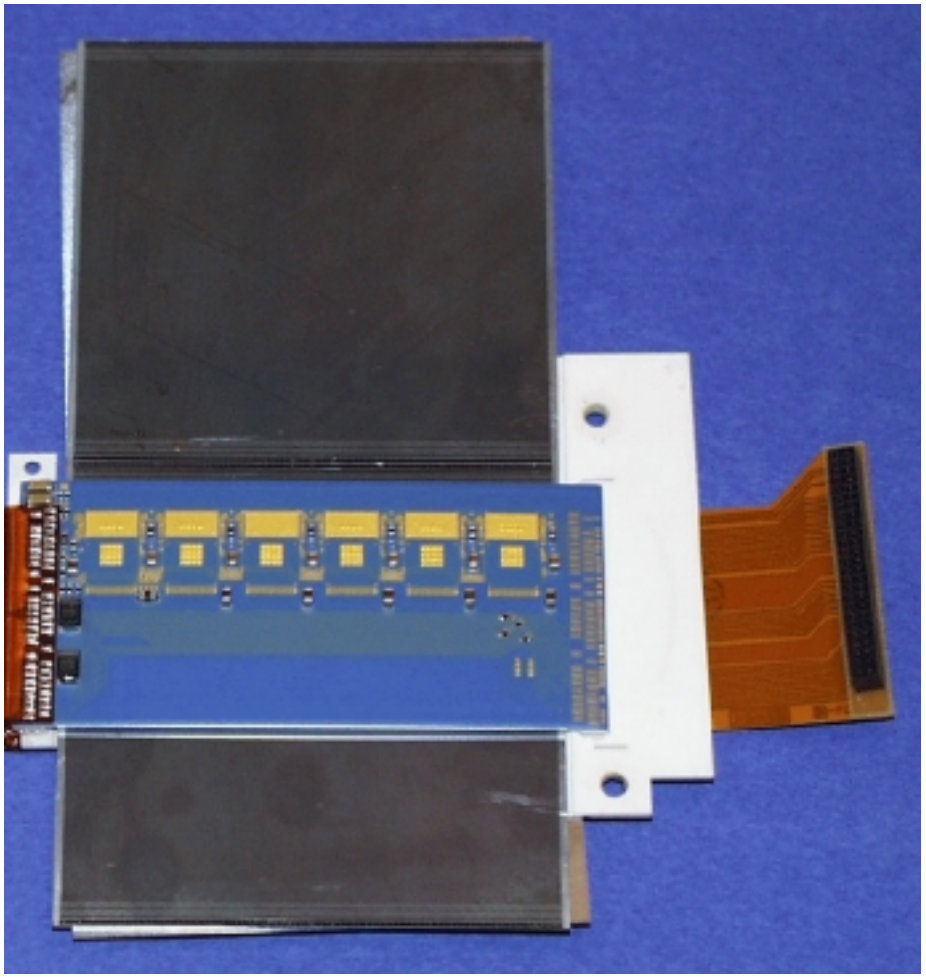
Silicon Strip Hybrids and Modules

- This year Atlas chose a hybrid techology based upon copper/kapton flexible circuits developed by the KEK group. Cost was the primary driver.
- These parts are fabricated in Japan.
- Samples have been distributed around the collaboration for tests and validation.
- We are in the process of studying these units here.
- Noise, stability, and interference are issues still to be fully demonstrated when FE chips are integrated into these modules.
- "Module 0" program in progress now.

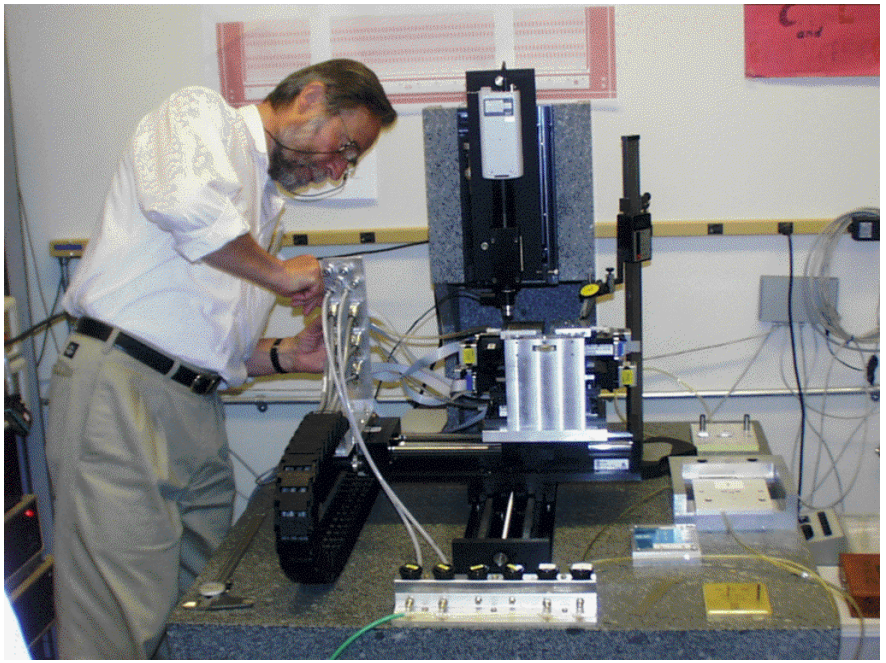
Barrel Silicon Strip Modules

Physics Division

Double-sided dummy module



- **Tooling for large-scale production(we have to assemble 700 modules)**
- **Practice(dummy) and few real modules built**
- **New tooling due this month**

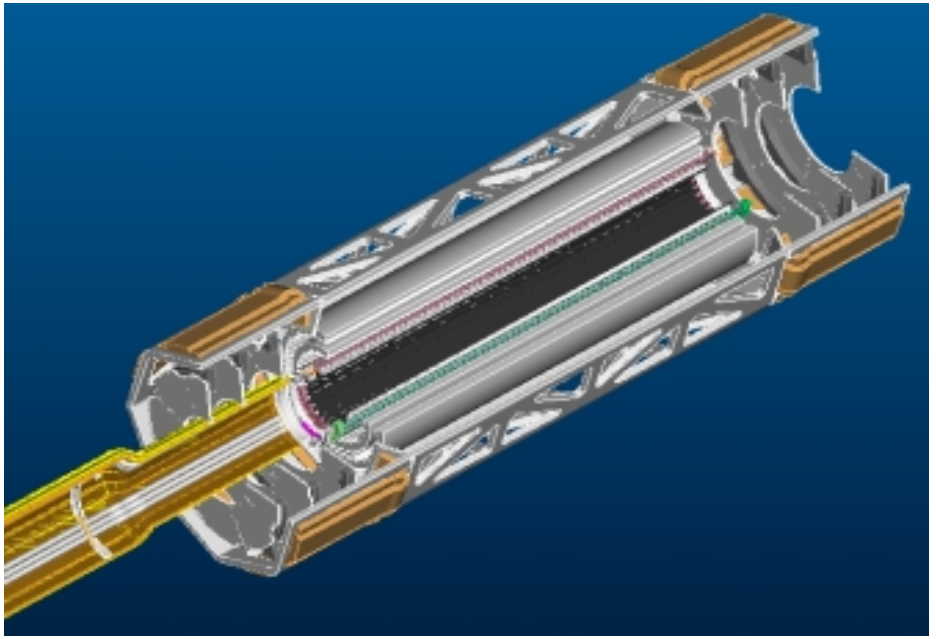


The ATLAS Pixel System

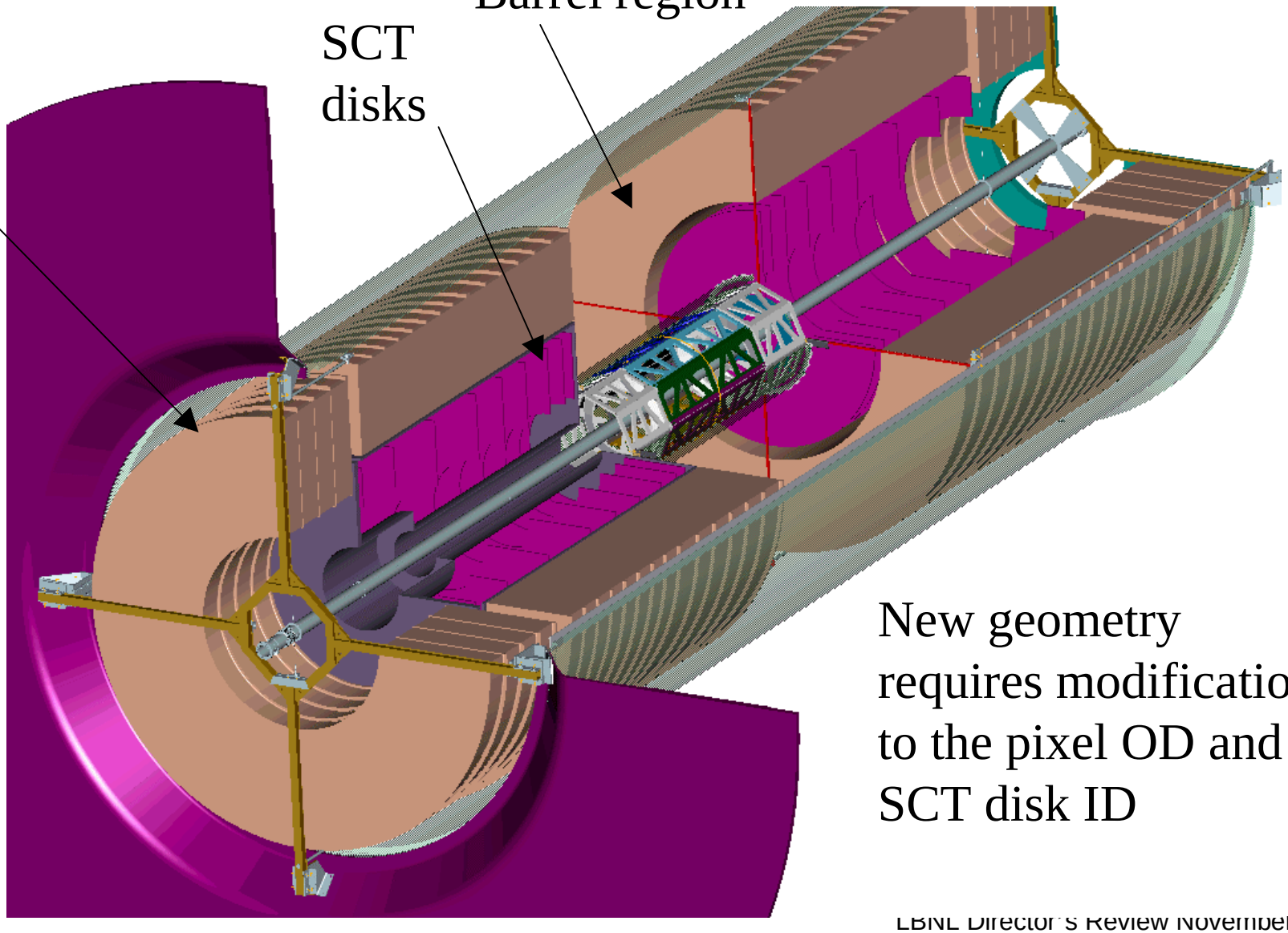
Physics Division

- **Layout**
  - 3 barrel layers, 2 x 3 disk layers
  - Three space points for |h|< 2.5
  - Modular construction(about 1800 modules)
- **Radiation hardness**
  - Lifetime dose - 50 MRad at 10 cm
  - Leakage current in 50μx300μ pixel is - 30 nA after irradiation.
  - Signal loss in silicon by factor 4-5 after 10^{15} n/cm^2)
- **Pattern recognition**
  - Space points. Occupany of - 10^{-4}
- **Performance**
  - Critical for b tagging(big physics impact)
- **Trigger**
  - Space points-> L2 trigger
- **B-Layer**
  - More demanding in almost all aspects
  - Evolving to essentially separate project

New technology in all aspects
=> prototype everything



Insertable Geometry



New geometry requires modifications to the pixel OD and the SCT disk ID

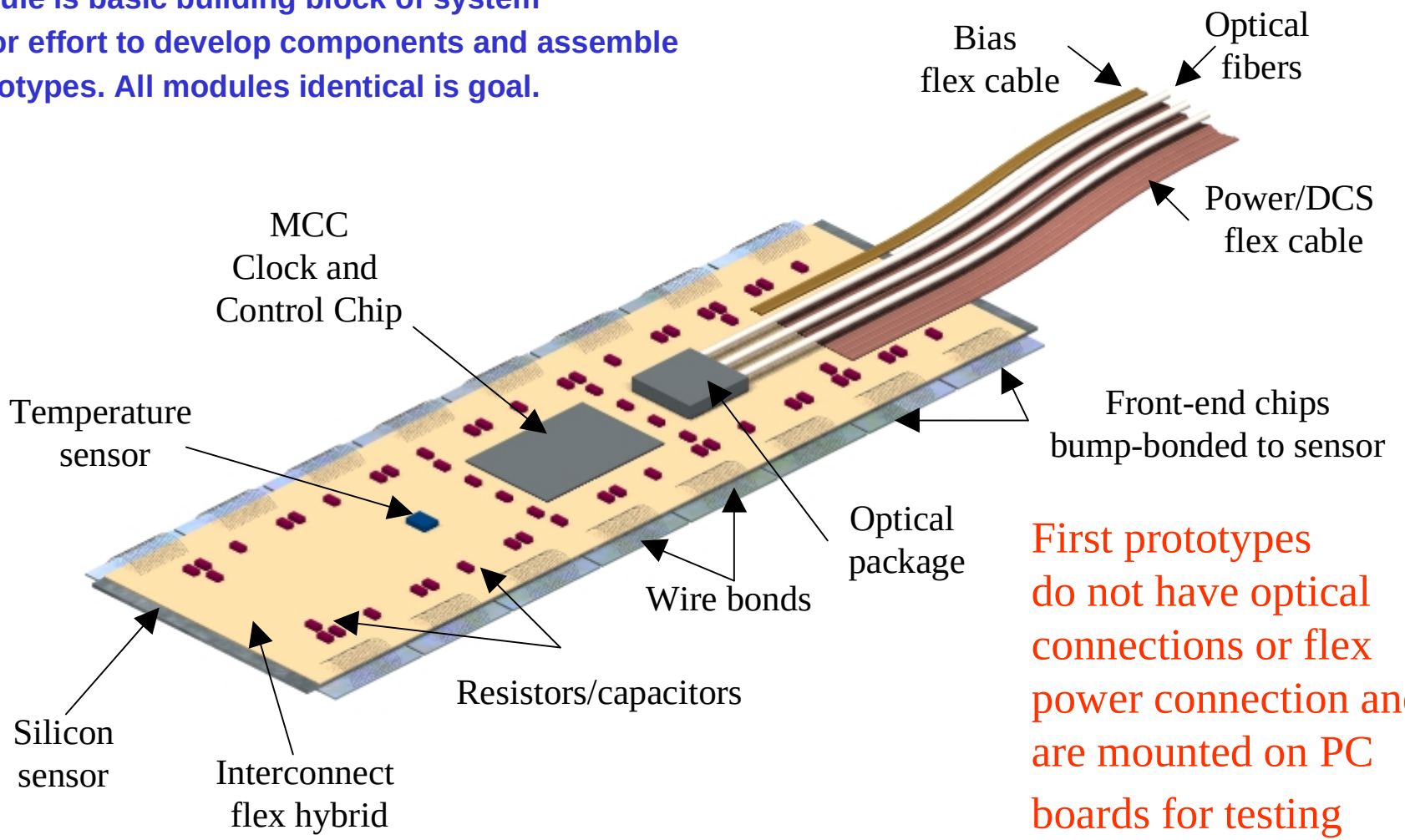
ATLAS Pixel System and LBNL

- **LBNL is involved in the following aspects of the Pixel System design**
  - Front-end integrated circuit electronics design and testing(K. Einsweiler is electronics coordinator for Pixel Collaboration)
  - Module design and assembly
  - Mechanical design of the disk and overall support.
  - Mechanical system integration.
  - Irradiation of electronics, detectors and mechanical components (mostly at the 88□ cyclotron but also in Cobalt sources at LBNL and LLNL)
  - Test beam and bench data acquisition and software
  - Test beam analysis
  - Development of pixel hybrid circuit.
- **Production responsibilities will be**
  - IC electronics (probe 50%, provide test system- 20 units)
  - Module construction and testing (25% disk and barrel)
  - Mechanical construction of the disk system, overall support frame and other parts of the mechanical structures.
  - Systems integration (in part) particulary of services, fabrication of low mass cables.

Pixel Module

Physics Division

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical is goal.

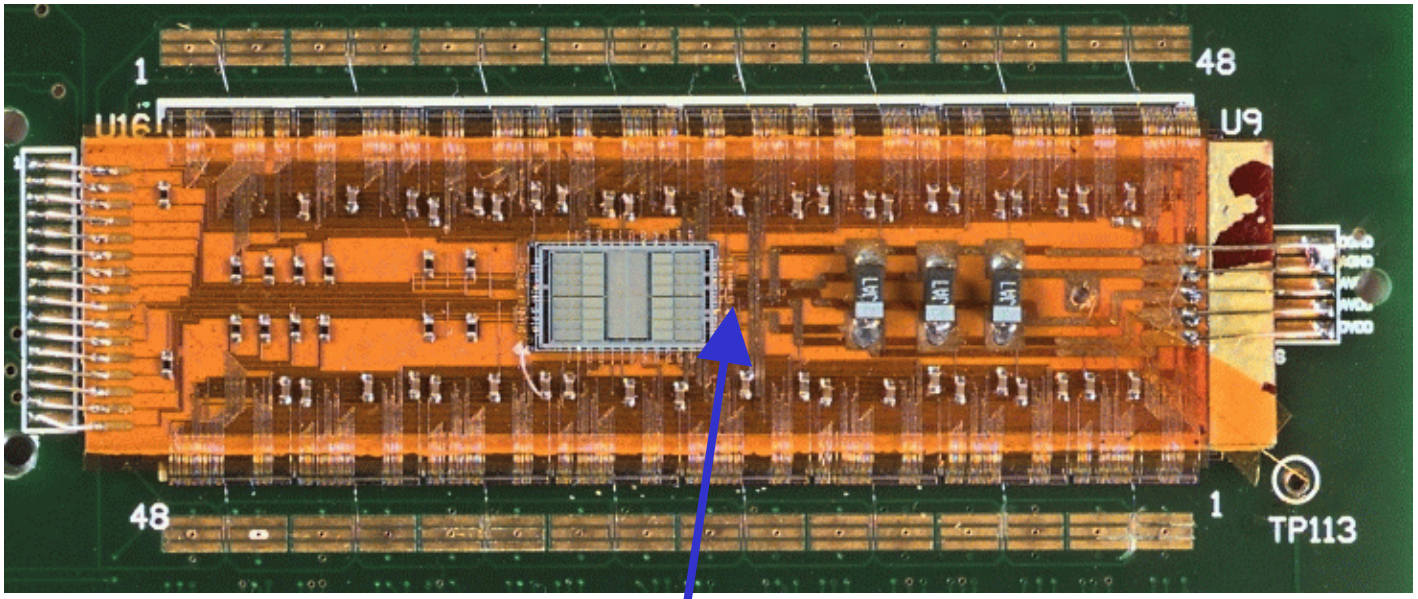


First prototypes do not have optical connections or flex power connection and are mounted on PC boards for testing

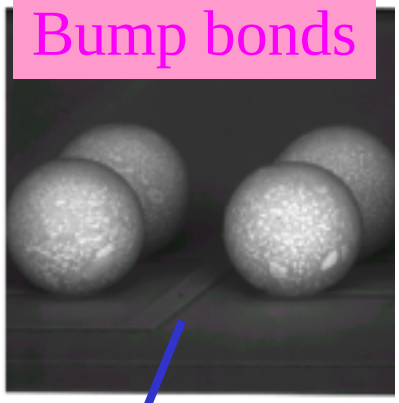
Pixel Modules

Physics Division

Module with flex hybrid and controller chip on PC board



Bump bonds

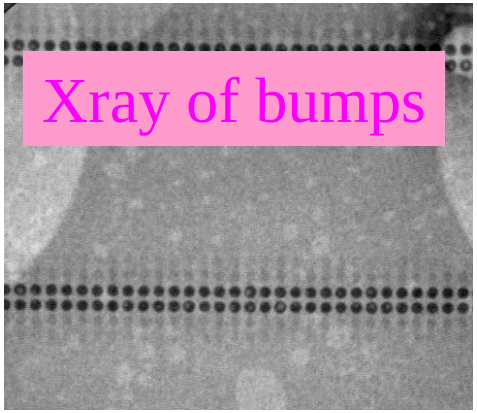


16 chips with 46,000 bump bonds

Sensor

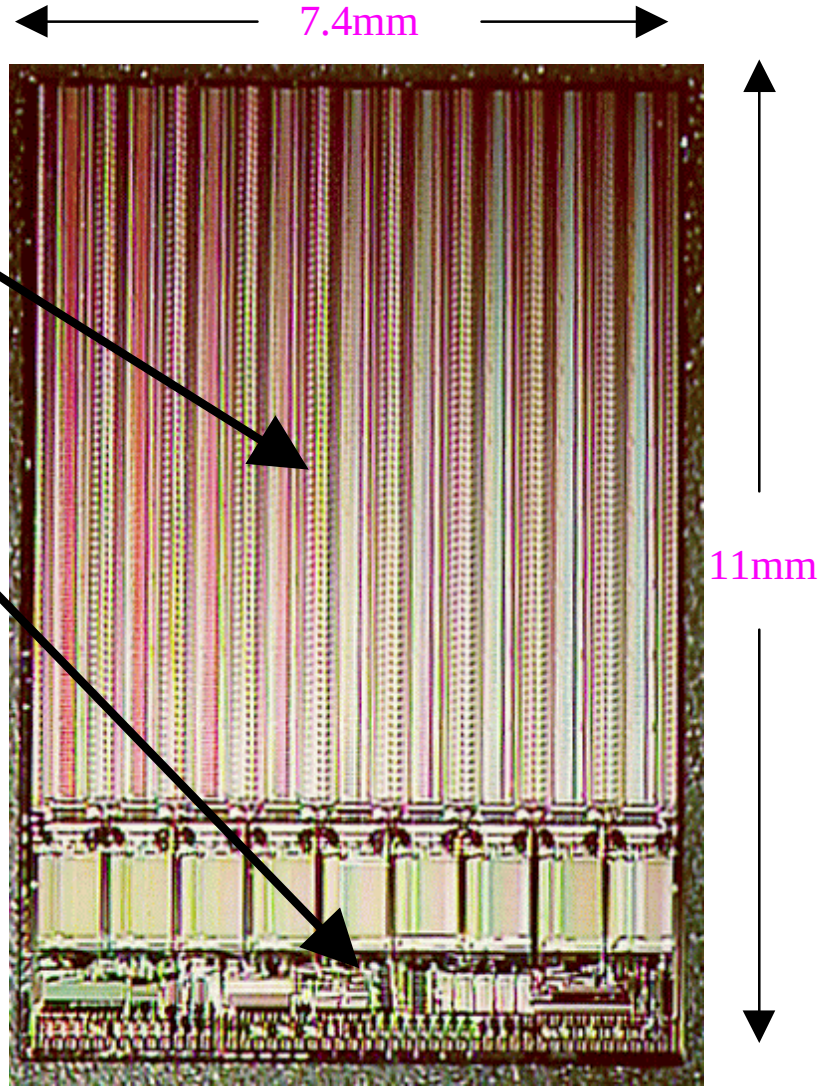
ICs

Xray of bumps



Pixel Electronics

- **General features**
  - Active matrix 18x160 pixels. 50x400 microns except in B-layer, which is 50x300.
  - Inactive area for buffer and control
- **Critical requirements**
  - Time walk <20 ns
  - Timing uniformity across array(<few ns)
  - Low threshold(2-3K e^-s)
  - Threshold uniformity (implemented by having DAC in each pixel)
  - Low noise(<few hundred e)
  - Low deadtime(<1% or so)
  - Robust(dead pixel OK, dead column not good, dead chip bad)
  - All of the above at 25 Mrad or more
- **Important requirements**
  - Time-Over-Threshold(TOT) measurement of charge
  - Maximize active area
  - Die size with acceptable yield
  - Thin(150 micron goal)



Lab and Test Beam Results - Summary - the good news

- Extensive lab tests, test beam runs at CERN from 1998-2000.
- Highlights
  - Rad-soft ICs tested so far (3 variants used - FE - A, - B, - C)
  - Dozens of single-chip/detectors have been operated successfully with multiple detector types and front-end ICs
  - 16 chip modules have been operated successfully
  - Detectors irradiated to lifetime fluence expected at LHC(10^{15}) have been read-out in a test beam with efficiency near 100%
  - Operation below full depletion voltage demonstrated
  - Preferred detector type chosen, based upon these studies
  - Timing performance needed to identify bunch crossings has been demonstrated, albeit not at full system level.
  - Operation at thresholds 2,000-3,000 electrons demonstrated
  - Threshold uniformity demonstrated.
  - Spatial resolution as expected
- Conclusion
  - Proof-of-principle of pixel concept successful

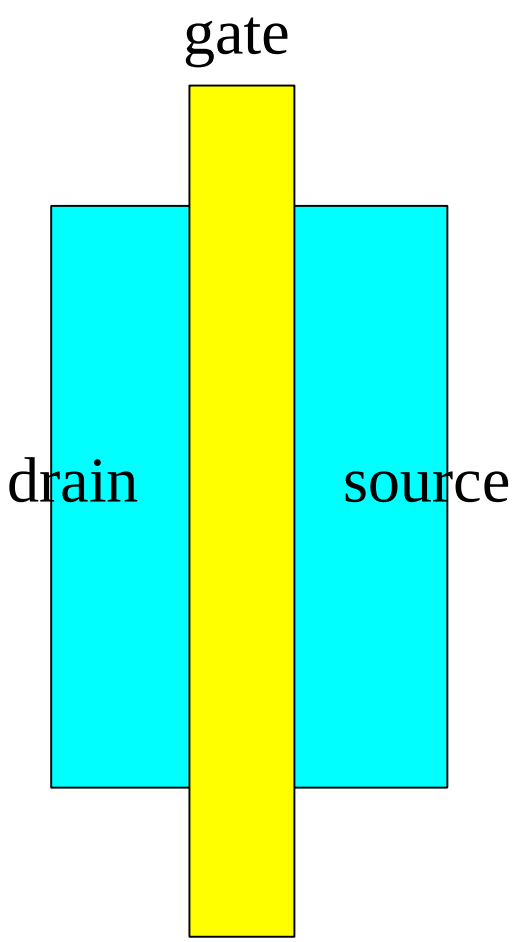
Rad Hard Electronics

- Rad hard development effort started 1998
- Pursue 2 vendors Temic (DMILL) and Honeywell (HSOI4)
- FE-D received 10/99 - Very poor yield
  - Significant study of yield problem - it is due to technology not design.
  - Noise higher than expectations on usable channels
  - Discussions with vendor, 2nd batch run but no significant improvement. Some theories to account for process problem
  - Another batch in process now, delivery 11/00, with additional design restrictions to avoid yield sensitive circuit elements
- FE-H design began 9/99
  - More flexible process, various improvements added
  - Implemented, in part, using high level digital design tools
  - 8/00 vendor quotes indicate x2.5 price increase -**effort terminated**

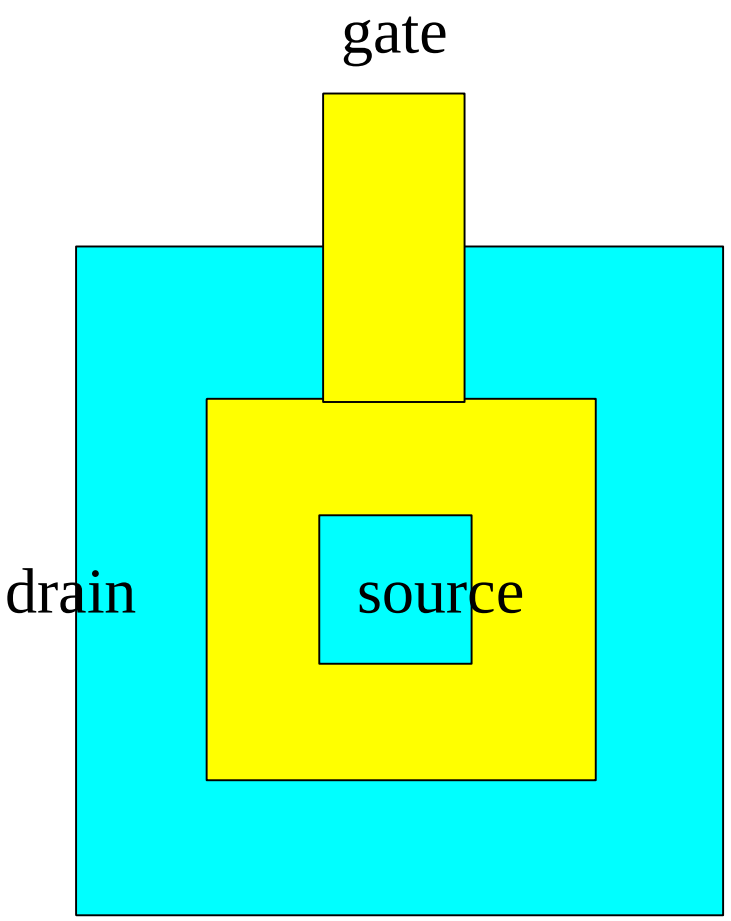
Deep Submicron Approach

- Many commerical foundries now offer 0.25 micron CMOS process (IBM, TSMC, UMC, CMC)
- RD-49 effort at CERN has shown that this technology can be intrinsically rad-hard
  - Thin gate oxides (~10 nm) lead to less charge generation and charge traps are neutralized due to tunneling
  - Thin gate oxides lead to other performance gains
  - Thick field oxide can lead to leakage but this is cured with enclosed transistors.
  - Wide use/interest in this process within HEP now
- Decision to develop new FE-I aimed at IBM process.
- Three designers active at LBL on this effort now.
- Submission planned for June 2001.

Deep submicron modification



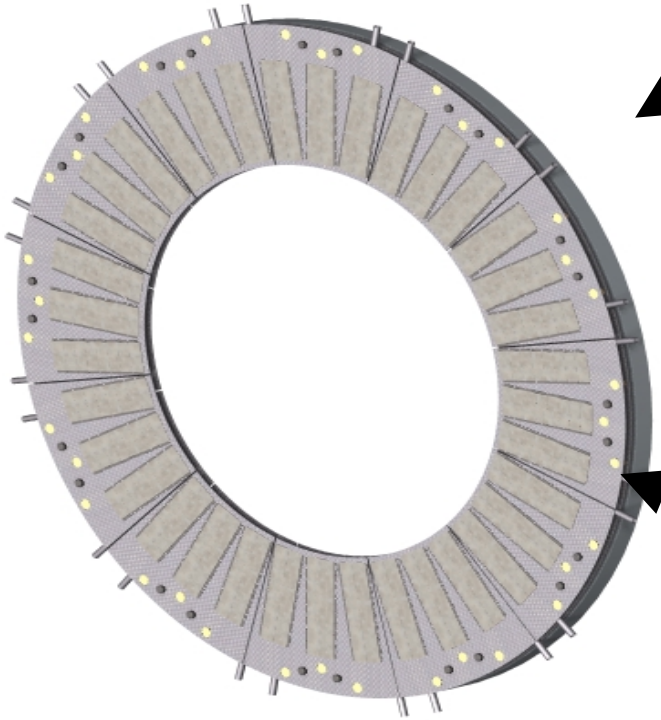
Traditional MOSFET

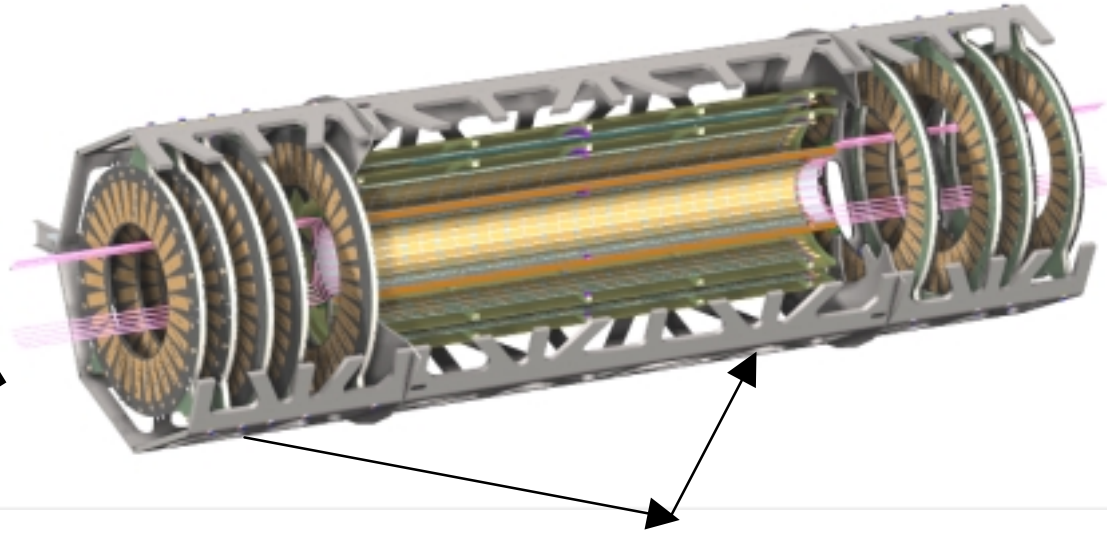


Rad Tolerant MOSFET

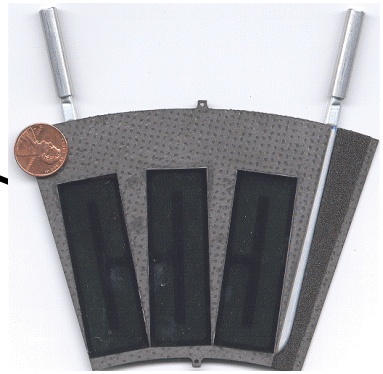
Pixel Mechanics

Coolant lines





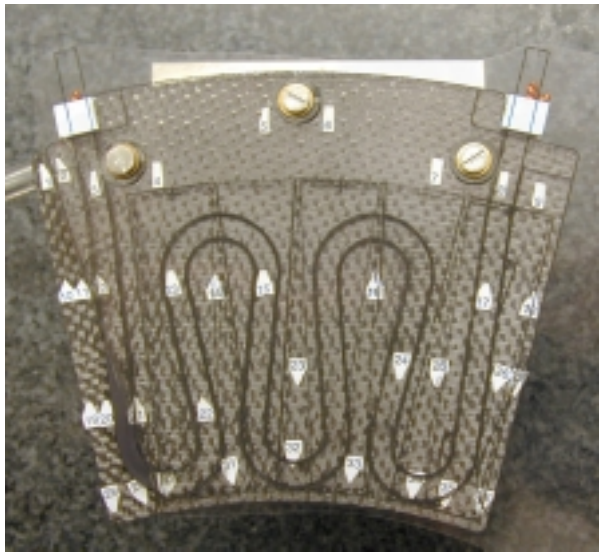
Support frame



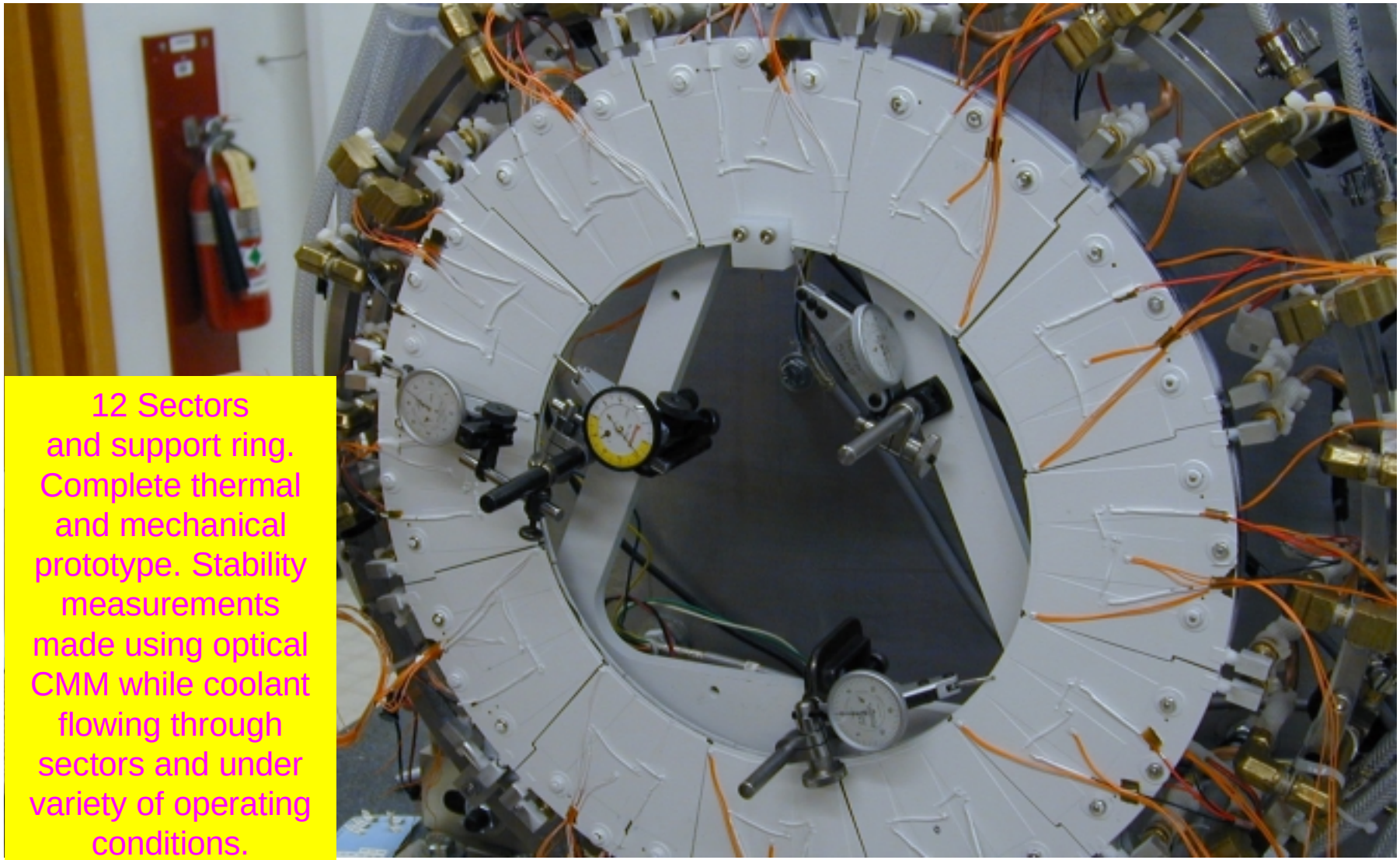
Sector- local support of modules

Baseline Sector Concept

- Combined structural support with cooling.
- Carbon-carbon faceplates. Front and back faceplates offset in phi to provide full coverage(minimal gaps).
- Aluminum coolant tube between faceplates.
- Three precision support points to disk ring.
- Modules mounted on both sides.

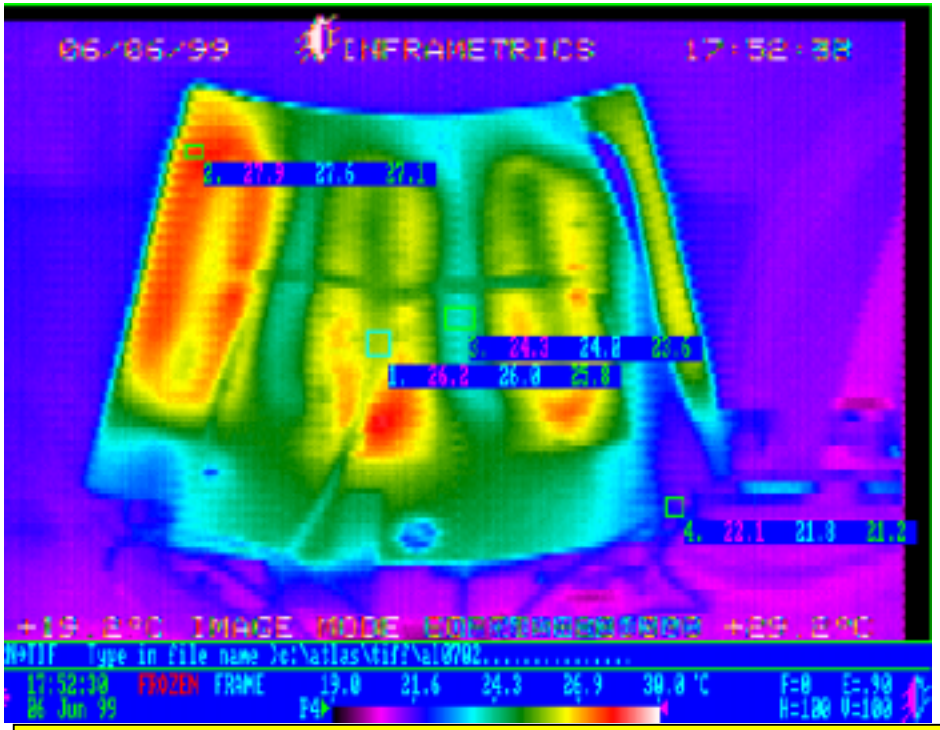


1st prototype disk

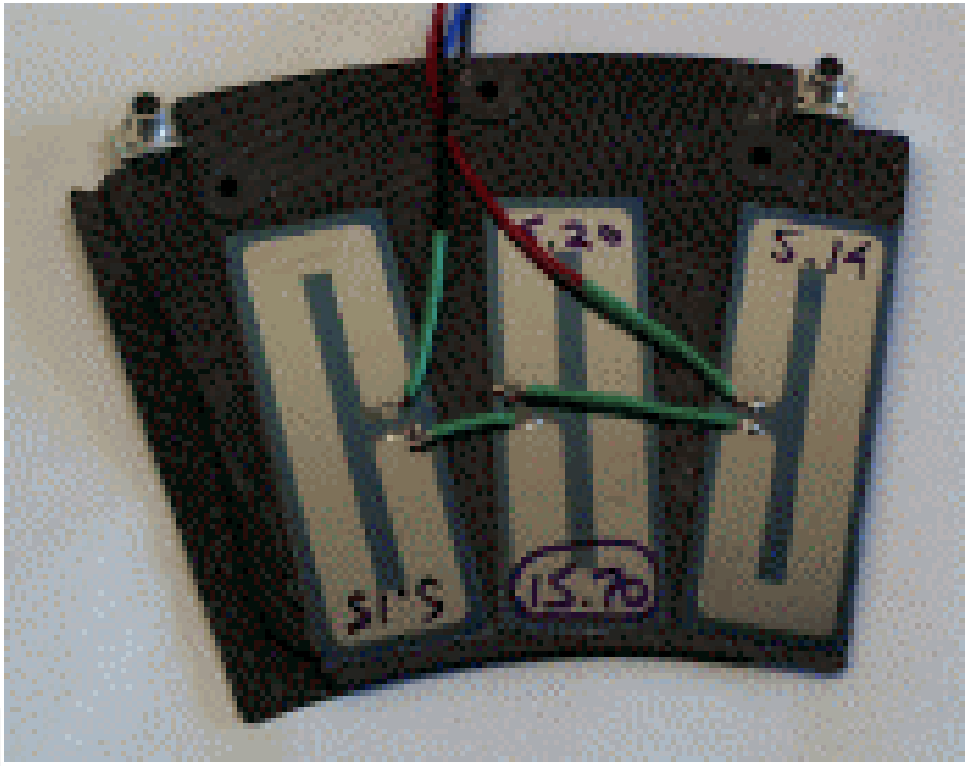


12 Sectors and support ring. Complete thermal and mechanical prototype. Stability measurements made using optical CMM while coolant flowing through sectors and under variety of operating conditions.

Thermal measurements



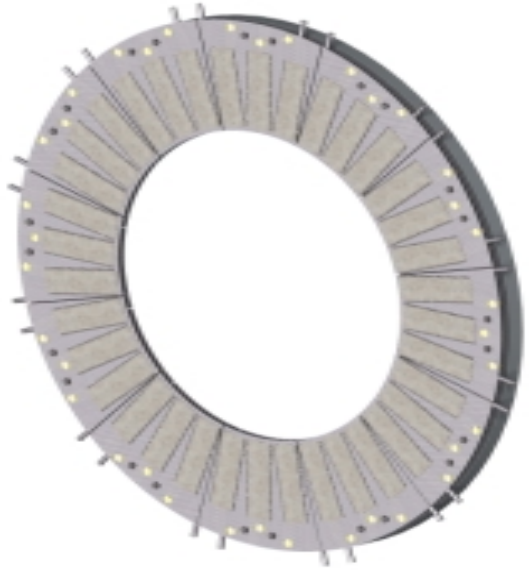
Infrared thermography has been used to assess thermal performance of sectors. This is a typical example of thermal performance using room temperature liquid cooling. Good correlation observed between ΔT seen in such tests and ΔT measured using baseline evaporative C_3F_8. IR thermography will be used in production QA.



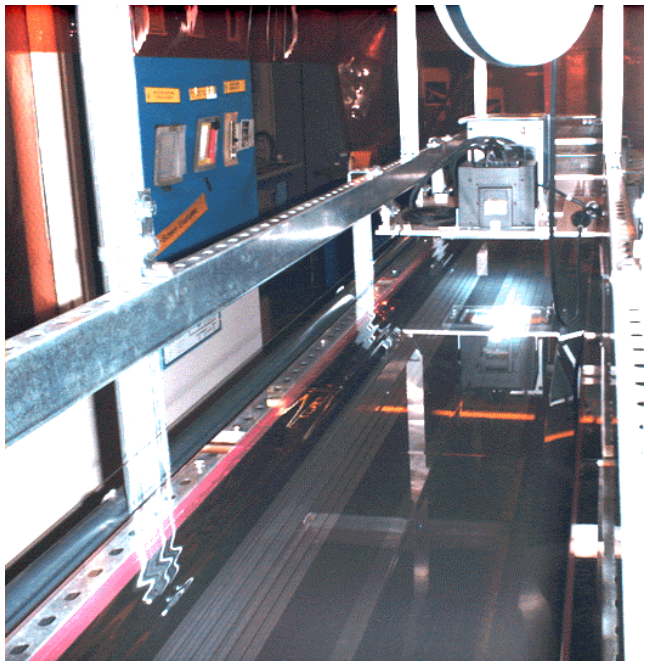
Platinum on silicon heaters to simulate heat loads. These are attached using the current baseline thermal material CGL7018. RTDs are also mounted to measure temperature at points and compare with IR images.

Disk Prototype

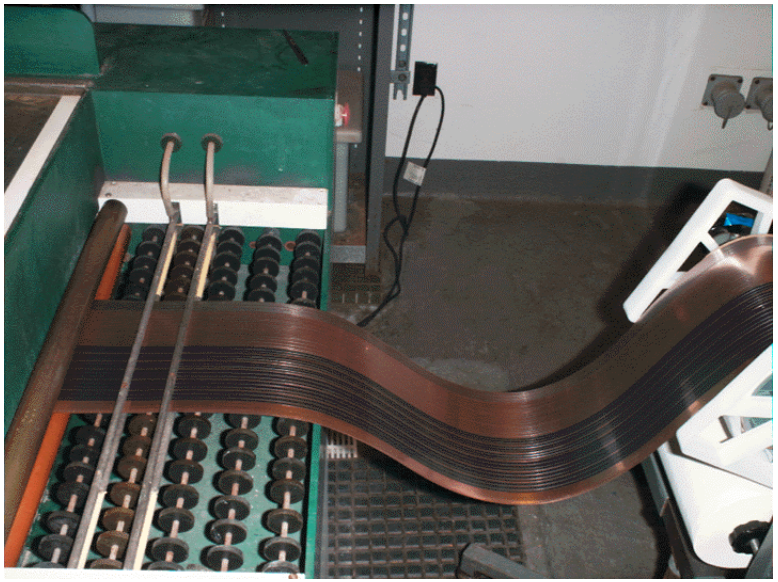
- Two full-disk mechanical and thermal prototypes have been made
- Assembly complete with 12 prototype sectors and disk



Prototype cable fab



- LBL responsible for low mass cables
- Flex Cables being produced at LBNL
- Wire partly purchased
- Artwork has All cable types in low mass bundles
  - Types I&II power, Mintrace, HV
- Prototype effort started with copper
  - Copper remnants from STAR OFC
  - Shop really geared for Copper
  - quickly prove out staging and production aspects



Computing and Physics

- Computing activities
  - Architecture and Framework
  - Applications
- Physics activity

Architecture and Framework

- Overall ATLAS co-ordination by Architecture team
  - 6 members - Quarrie, Tull, and Calafiura from LBL, Quarrie appointed Chief Architect in March 2000
  - LBL has lead responsibility for ATLAS framework (ATHENA)

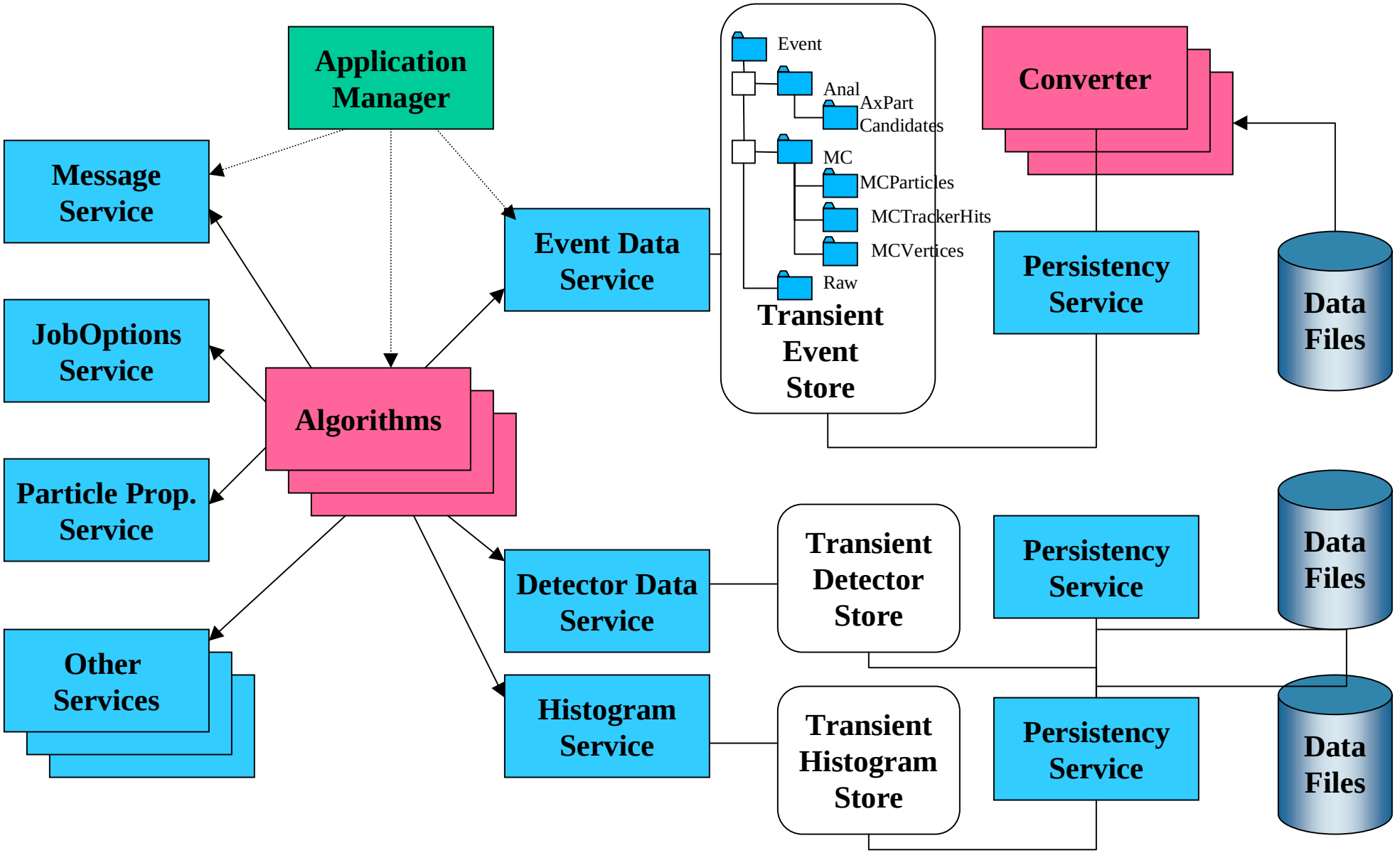
New Framework

- New Object Oriented Control Framework
- Used by all off-line activities: simulation, reconstruction, physics analysis and in Event Filter (=Level 3 Trigger)
- Urgent, critical path for all software activities
- Functional version must be available by end 2000
- Decided to adopt LHCb (GAUDI) framework as starting point
- Workshops held at CERN in March and April.
- Review committee established July 2000, has tried to redefine milestones. Expected to endorse approach shortly.
- Used Unified Software Development Process (USDP) using Rational Rose suite for Reverse engineering, user requirements and diagnostics.

Basic Functionality

- Data read from permanent storage into transient data store
  - + System is independent of choice of database.
  - + Converter maps from persistent store to transient
- (intelligent) Data objects accessed by users from transient store
- Algorithms controlled by the framework and act on data
  - + e.g.Pattern recognition, event simulation, Higgs analysis. Written by users, initialized and executed by framework
- Services are globally available components that can be used by Algorithms
  - + e.g. Histogram, visualization, random numbers
- Properties are control and data parameters
  - + e.g. width of road used for track finding

GAUDI object diagram



May Milestones

- All essential deliverables met, Only one optional deliverable missing, delivered several items not on the original list
- Partial list
  - Demonstrate system with basic functionality — Met
  - Make system available to developers on one platform — Met
  - Ability to access existing (FORTRAN generated) simulation data — Met
  - Ability to execute sequence of User Modules — Met
  - Ability to read/write from Transient data store — Met
  - Allow incorporation of existing modules with minor change <10 lines — Met
  - Provide tutorial for application writers. Given at LBNL during May software week, repeated at CERN twice (70 attendees total) — Met
  - Demonstrate incorporation of some existing software packages — Met
  - Generate Event Display (not primary LBNL deliverable) — Met
  - Ability to execute sequence with branches and filters } — Met
  - Dynamic loading of Modules (Sufficient for developers) — Met
  - Limited data persistence (HBOOK) — Met
  - Rudimentary interactive interface — Not yet

September Milestones

- **All essential milestones met**
- **Athena made available to collaboration (LBL)**
- **Event Generators (LBL) and prototype Fast simulation (UCL) released**
- **Prototype scripting interface (LBL)**
- **Physics analysis output to ROOT and PAW (LBL)**
- **Test beam data input from Objectivity**
- **Auditor Prototype (LBL)**
- **Dynamic loading with common executable**
- **Event Data Model (LBNL/BNL)**
  - **Provides interface to data in Transient store**
  - **Access to data from User Algorithms**

Applications in new Framework

- Histogramming/NTuple service (Leggett)
- LAr reconstruction code imported in 2 days
- (S. Rajagopalan, BNL)
- XKalman++ pattern recognition package operational (Vacavant)
- Physics generators. New package to load events into transient store. Some functionality now. Full functionality by Sept (Hinchliffe, Shapiro)
  Prerequisite for new fast simulation (UCL deliverable)

Future Framework Activity

- **December 2000: Full reconstruction available**
  - Pile up support demonstrated
  - Full input from Geant3 simulation
  - Detector description prototype
  - Fast Simulation deployed (not validated)
  - Event Data Model deployed
  - Binding to JAS and ROOT demonstrated
- **April 2001**
  - Features freese for full version
  - Objectivity I/O deployed
- **Sept 2001: First full version**
  - Ready for Mock Data, starts end 2001
- **April 2002: Full version with distributed capability**

Physics Activities

- Physics Technical Design report issued last year
  - http://atlasinfo.cern.ch/Atlas/GROUPS/PHYSICS/TDR/access.html}
- Documents performance of ATLAS for a wide range of signals
  - Higgs, Supersymmetry, QCD, B-physics
- Some physics studies continuing, needed to ensure compatibility with new theoretical developments, trigger strategies
- Discussion of possible LHC upgrades
  - Luminosity increase by factor of 10?
  - Double Energy?
  - Former is very limited due to pile up and detector problems
  - Latter doubles reach and gives ten times rate for most new discoveries

Summary

- SCT effort is nearing a production phase
- Pixel effort
  - Mechanical effort is in excellent shape
  - Major contributions to the electronics, group is playing a leading role, deep submicron effort will be a challenge but is key to the project
- Computing
  - Outstanding effort on the new Framework
  - All milestones are being met
- We have received critical infrastructure support from the Lab and the Directorate and we look forward to continued support as we approach the production phase of the project.